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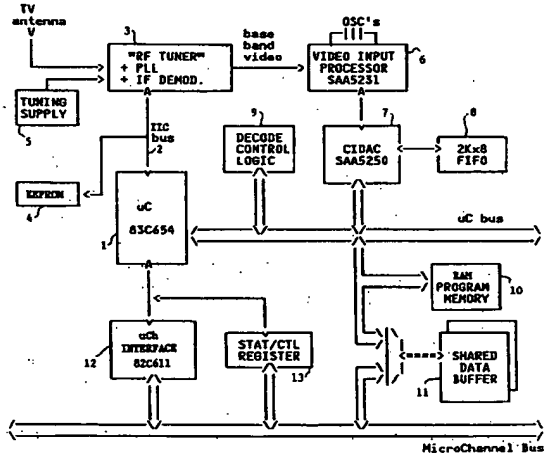
(54) Selective data broadcasting receiver adapter for personal computers.

(57) The present invention relates to a microcontroller based adapter card that interfaces a Microchannel bus architecture to allow a personal computer implementing such hardware architecture to tune on a TV channel and capture digital data transmitted intermixed with an analog video signal used for diffusion of television programs. The receivers of such transmission system receive the incoming data stream, transmitted via "on air" or "cable" channels, through a TV cable of a broadcasting network or from the aerial antenna. Received serial data is decoded and stored into byte format for processing which is partially done by the on-board processor and then by the personal computer processor. This processing will result in storing data as records, messages and files formats into the personal computer mass storage devices. The on-board intelligence allows selectivity of transmitted data by checking the incoming addressing bytes (transmitted in the same data packet) against the card unique address or group membership parameter stored in non-forgeable devices.



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The invention applies to the field of data transmission based on an unidirectional broadcast system and more specifically refers to an adapter which implements the receiver function of the system.

The subject adapter consists in a microcontroller based card that interfaces a Microchannel bus architecture to allow a personal computer using such architecture to tune on a TV channel and capture the digital data transmitted with the analog video signal.

The physical data transmission means is the unidirectional broadcasting system used for diffusion of television programs. The receivers of such transmission system receive the incoming data stream, transmitted via "on air" or "cable" channels through a TV cable of a broadcasting network or from the aerial antenna.

According to the present invention the received serial data is decoded and stored into byte format for processing which is partially done by an on-board processor and then by the host. This processing will result in storing data as records, messages and files formats into the personal computer mass storage devices.

Data consists of a plurality of variable length messages from one or many information-providers to one or more end-users over a broadcast or multicast transmission system.

The on-board intelligence allows the selection of transmitted data by checking the incoming addressing bytes (transmitted in the same data packet) against the card unique address or group membership parameter stored in non-forgeable storage.

This process refers to a general "selectivity scheme" implemented in a given transmission protocol which is intended to give the information-providers the ability of addressing each single end-user or grouping any subset of those end-users which are likely receiving the same data.

The addressing selectivity is dynamically modifiable by the remote information-provider by sending control packets to explicitly enable/disable the receiving capability of the adapters as well as explicitly change the end-user group membership.

The above-mentioned "selectivity scheme" is also described in the co-pending European Patent Application titled "Selective data distribution method using unidirectional broadcast or multicast transmission" filed by the same Applicant.

US-A-4,829,569 discloses a subscription television system in which individual decoders are enabled to receive individually addressed messages. However, the cited prior art patent does not teach how to organise for a selective transmission of data and how to selectively receive such data. According to the prior art, individual decoders in a subscription television system can be addressed for transmission of either billing information or individual messages; this suggests only a distinction between transmission directed to a single addressee and a broadcasting transmission. The same scheme may be applied to non subscription television, substituting the decoders with a special-purpose device.

It is therefore an object of the invention as claimed to overcome the above drawbacks of the prior art.

For a better understanding of the present invention, together with other and further advantages and features thereof, reference is made to the following description and to the accompanying drawing, the scope of the invention being pointed out in the appended claims. The figure shows a block diagram of the data broadcasting receiver board according to the present invention.

HARDWARE DESCRIPTION

The adapter hardware is specifically conceived to be interfaced to a personal computer Microchannel bus architecture and fits into the subcategory of an "8-bit Slave Adapter" implementing all the related logic like Programmable Option Select registers, Addressing and Interrupt systems, Card Setup mechanism (all characteristics of the Microchannel bus architecture). On the other side a hardware set for Teletext based applications is implemented to allow direct connection to coaxial cables carrying the RF-Video signal where digital data is intermixed. Typically this cable comes from a TV antenna or a cable TV network. This set of devices including the RF Tuner, IF demodulator, Teletext Video Processor and Data Decoder C.I.D.A.C. (manufactured by Philips) represents the 'Front-end hardware' as called in the following description. A tailored amount of memory is available on the board with the purpose of storing the adapter code (Program memory), the received and processed data bytes (Data Buffer) and nonvolatile data for user selectivity and data protection (EEPROM).

With reference to the block diagram in the figure the following major functional blocks are described:

- The 83C654 single-chip 8-bit microcontroller (1), sold by Philips, is an advanced CMOS derivative of the 8051 microcontroller family. With respect to its originator 8051 core CPU, it has enhanced features like:
  16Kx8 ROM, externally expandable to 64K bytes. - 256x8 RAM, externally expandable to 64K bytes. - Two 16-bit timer/counters - Embedded IIC bus controller.
  The IIC feature (2) is particularly suitable for the present application because of the presence of two IIC bus compatible devices: Tuner PLL (3) and EEPROM (4).

The microprocessor is clocked by a 16MHz crystal that allows 58% of instructions being executed in 750 nsec. and 42% in 1500 nsec.

* The 'Front-end' hardware comprises :
  RF-Tuner (3) with PLL frequency synthesis which performs the function of tuning and demodulation of TV signal obtaining the base band video signal. A Tuning Supply (5) supplies the tuning voltage.
  Video Input Processor SAA5231 (6), (manufactured by Philips) which performs the extraction of digital data from analog composite video signal and the bit serialisation and synchronisation. This device has a free running oscillator driven by an external crystal of 13.875 MHz which is twice the frequency of the received bits.
  C.I.D.A.C. Decoder SAA5250 (7) having the function of recognising and storing the bit streams belonging to the desired logic channel. It is programmable by the 83C654 processor (1) for different types of communication protocol standards.
  C.I.D.A.C Decoder (7) stores the received data bytes into its local 2Kx8 FIFO memory (8).
  C.I.D.A.C. Decoder (7) has a private 2Kx8 FIFO memory (8) for received and decoded bytes. This memory is handled by the C.I.D.A.C. Decoder as a FIFO queue to allow the processor (1) to retrieve data in the same received sequence. Processor (1) has not access to FIFO memory (8), instead it reads the available byte from a register 'Fifodata' included in C.I.D.A.C. Decoder (7). It also checks the FIFO status (empty, data available, full) by reading the C.I.D.A.C 'Fifostatus' register.
* Control and Decode Logic (9) is the hardware logic having the function of decoding the addressing, controlling the transfer and other hardware functions.
* The on-board memory resources include a 32Kx8 RAM program memory (10) to extend the program space of processor (1) up to 48K bytes of total code area and two banks of 16Kx8 RAM Shared data buffers (11) to store intermediate packets and communication information between the on-board processor (1) and the host processor of the personal computer. The RAM program memory (10) gives the flexibility of code download for algorithms updating and maintenance aspects, while the Shared data buffers (11) allow concurrent operations of the two processors without stopping each other activities and also increase the buffer size in order to maintain receiving data throuput as high as possible.
  2Kx8 EEPROM (4) is the non-forgeable portion of the adapter memory resources for storing permanent information like unique hw-id, group-membership-id parameters and so forth. The above bytes must reside on the board to assure a sufficient level of protection for vital data on which the selectivity scheme is based upon. Only the on-board processor (1) has access to that data via the IIC bus (2).
* Most of the logic to interface the host Microchannel bus reside in the 82C611 chip (12), manufactured by Chips & Technology, which supports the following functions which are typical of the Microchannel architecture:
  - I/O and Memory slave adapters control logic.
  - Programmable Option Select (POS) support including :
    * Adapter ID
    * Flexible I/O and Memory relocation
    * POS port Decode and Handshaking - Command and Status decoding - Response signal generation - Full bus timing specification compatibility
* Status/Control Registers (13) are two resources accessed by the host processor to check the status and to control specific configuration transitions of the adapter hardware.
  The receiver board, according to the invention, implements a Slave type adapter in the sense that the memory resources and the Status/Control registers (13) are mapped into the personal computer memory space which is relocatable via the POS registers and the Adapter Descriptor File (ADF) facilities.
  This is the key way used by the user application programs for exploiting the on-board hardware resources by sending commands and retrieving the received data.

OPERATION OVERVIEW

The operation of the adapter is totally under control of the on-board processor (1) which receives commands from the user program, via the "application interface layer" of the transmission protocol, and executes these commands for receiving the desired TV channel, decoding the captured data and handling the error protection/correction bytes. These preprocessed data is then passed to the upper software layers for final processing.
The IPL and Power On Tests functions are handled by the code resident in the masked ROM of processor (1). High test coverage and failure isolation is achieved due to the processor access to almost all the functional devices. At the end of diagnostic tests the functional code is downloaded to the program RAM under control of the host computer

processor and the adapter enters the ready status for data reception. The host device driver code passes the required parameters to the adapter code that starts programming of the tuner PLL device (3) and C.I.D.A.C. decoder (7) to get the data from the desired TV channel and logical protocol link. Data streams (packets) are then retrieved from decoder FIFO (8) by processor (1) and error handling routines are entered by checking the 'Hamming-protected' and 'CRC-protected' bytes. This process implements the 'Data Link' algorithm. At this point the true functional processing of received bytes starts and the protocol 'Network layer' algorithm begins. This algorithm is based upon the card unique-id's and group membership parameters which are stored in non-forgeable way in EEPROM memory (4). The task is totally carried out by microcode which can reside on the adapter program RAM or on the computer host processor system memory. In any case the received packets are then passed to the software upper levels to finally present data to the user application. Hardware level synchronisation is obtained by the Interrupt mechanism in both directions, host to adapter and adapter to host, and by the status/Control registers (13). Beside this hardware resources it is possible to use a code level information exchange by means of shared data buffers (11) which are accessible by the two processors. On the base of this shared memory resource, called 'Communication Area' it is possible to implement a handshake mechanism for processors operation optimisation and synchronisation.

Claims

1. A personal computer (PC) adapter card for receiving data transmitted by a broadcaster in an unidirectional broadcasting system using a TV channel which transmits digitally encoded data according to a given protocol, said adapter card having:

   1) A device (3) for tuning and demodulating a TV channel signal;

   2) a device (6) for separating the digitally encoded data from the TV composite signal;

   3) a programmable device (7) for recognising, receiving and storing said received data;

   4) a memory (4) non-forgeable by the end-user for storing information;

   5) a processor (1) for controlling said devices (3), (7), for programming said memory (4) and for processing said received data;

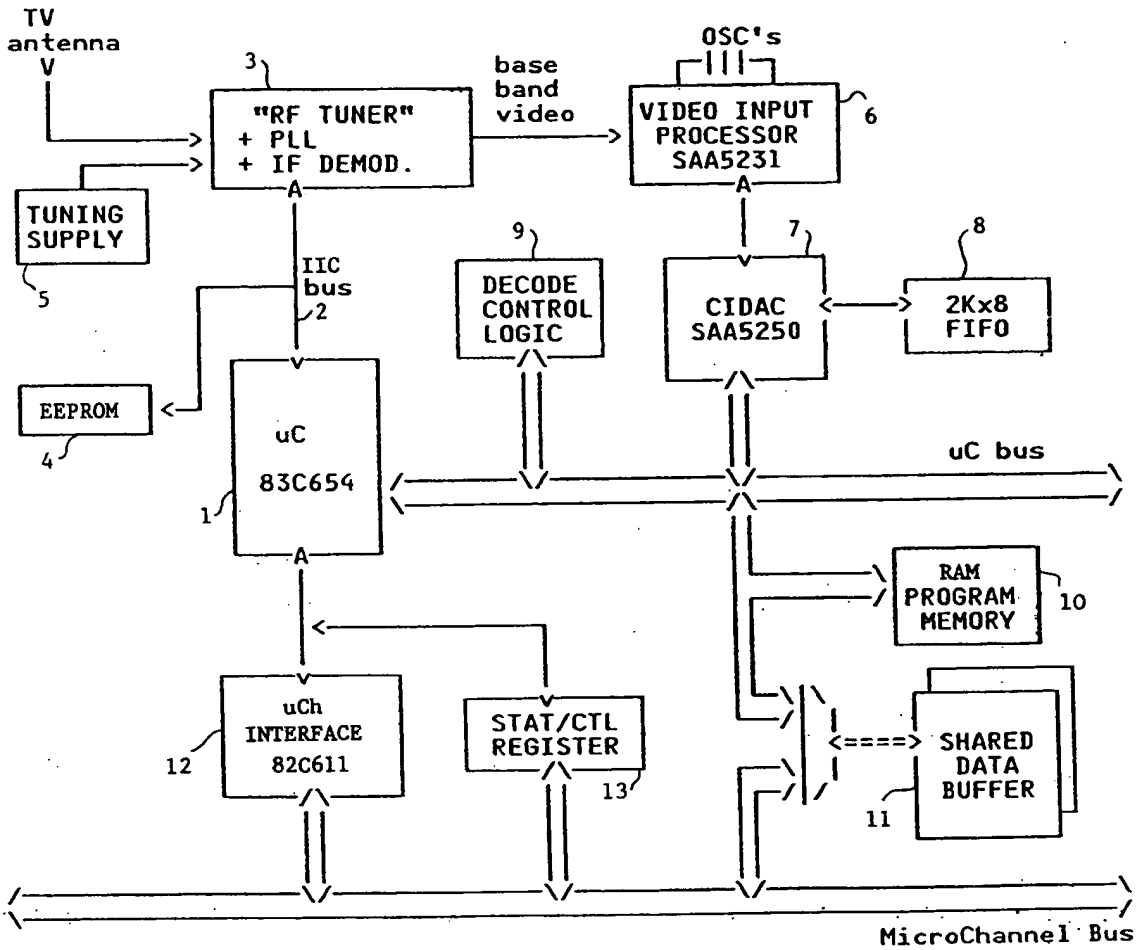
   (6) a data buffer (11) for storing said received data and communication information between said processor (1) and the host processor of the personal computer;

   said adapter card being characterised by the fact that:

   said device (7) is a decoder programmed to recognise and receive data transmitted according to a given communication protocol; said memory (4) is forgeable by said broadcaster and stores unique information relating to a selective transmission directed to said end-user or to a group of end-users wherein it is included;
   said data buffer (11) allows concurrent operations of processor (1) and PC processor and increases the data receiving throuput.

2. A method for selectively receiving digitally encoded data transmitted by a broadcaster in an unidirectional transmission system using a TV channel including the following steps:
   - tuning a selected TV channel;
   - programming a decoder (7) for a given transmission protocol;
   - storing and updating unique parameters relating to a selective transmission according to a given transmission protocol;
   - retrieving received data from said decoder (7);
   - checking addressing data against selectivity parameters stored in a memory (4) non-forgeable by the end-user;
   - performing error detection/correction;
   - storing final data in a data buffer (11) for upper software layers operations.

3. Adapter card as claimed in claims 1 and 2 further characterised in that said personal computer uses a Microchannel bus architecture.


TV
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12
STAT/CTL
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SHARED
DATA
BUFFER
11
MicroChannel Bus

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 12 4488

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	EP-A-0 306 208 (RAI) * Column 6, line 36 - column 12, line 14 *	1,2	H 04 N 7/08
A		3	
Y	US-A-4 058 830 (Y.M. GUINET et al.) * Column 2, line 29 - column 3, line 32 *	1,2	
A	BBC RESEARCH DEPARTMENT REPORT, no. 10, August 1988, pages 1-18, BBC, Tadworth, Surrey, GB; D.T. WRIGHT: "Conditional access broadcasting: Datacare 2" * Page 3, paragraph 3.1; page 6, left-hand column, line 24 - page 15, left-hand column, line 12 *	1,2	
A	EP-A-0 078 185 (TDF) * Figure 5; page 13, line 15 - page 14, line 12; page 20, lines 4-9 *	1-3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 04 N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	08-07-1991	BOSCH F.M.D.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
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